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AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph starting on page 15, line 14 with the following amended paragraph:

The model 300 includes a first and a second mixing nodes 304, 310 a first and a second summing nodes 306, 316, a gain impulse response 312, and a group delay impulse response 314. The first and the second mixing nodes 304, 310 mix an observation signal 302 with a first and a second oscillator signals 320, 322, respectively. The first oscillator signal 320, indicated by $cos(\omega_c t-\theta_c)$ includes a phase deviation θ_c, which simulates the phase difference between the LO signal 176 applied to the AQMS 104 and the phase shifted LO signal 178 applied to the AQDS 110. The second oscillator signal 322, indicated by $-sin(\omega_c t-\theta_c+\Phi_d)$ is at about 90 degrees of phase lag relative to the first oscillator signal. The Φ_d term accounts for a constant deviation from the ideal 90 degrees of phase lag that exists in actual systems.

Please replace the paragraph starting on page 25, line 23 with the following amended paragraph:

The first in-phase adder 1026 sums the output of the in-phase DC offset register 1010 with the in-phase portion of the received baseband signal 160 to remove the DC offset introduced by the AQDS 110. The ~~second in-phase~~ first quadrature-phase adder 1028 similarly sums the output of the quadrature-phase DC offset register 1012 with the quadrature portion of the received baseband signal 162 to remove the DC offset introduced by the AQDS 110. Of course, DC offsets present in the received baseband signal 160, 162 can also be removed by summation at a different point, such as at the second in-phase adder 1038 and the second quadrature-phase adder 1044. When the termination switch 108 selects the sample signal 144 as the observation signal 148, DC offsets measured at the received baseband signals 160, 162 or the demodulated baseband signals 164, 166 include offsets from both the AQMS 104 and the AQDS 110.

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Please replace the paragraph starting on page 27, line 3 with the following amended paragraph:

The output 1034 of the I-to-I compensation filter 1002 and the output 1036 of the Q-to-I compensation filter 1004 are summed by the second in-phase adder 1038 to provide the in-phase demodulated baseband signal 164. Similarly, the output 1040 of the I-to-Q compensation filter 1006 and the output 1042 of the Q-to-Q compensation filter 1008 are summed by the second quadrature-phase adder 1044 to provide the quadrature-phase demodulated baseband signal 166. Exemplary impulse responses that characterize the compensation filters 1002, 1004, 1006, 1008 are described later in connection with Figures 11 and 12.

Please replace the paragraph starting on page 34, line 23 with the following amended paragraph:

Figure 14 illustrates signal leakage characteristics of a portion of the phase shifter 114. In a first position, the first and the second switches 1302, 1304 select the first path 1306. Most of the input signal to the phase shifter 114, the LO ~~output~~ signal 176 from the local oscillator 116, follows the first path 1306 as indicated by dashed line 1406. However, a relatively small amount of the input signal to the phase shifter 114 leaks through other paths, such as the second path 1308, which is indicated by dashed line 1408, even when the second path 1308 is not selected. Sources for signal leakage include leakage through switches and coupling across conductors. For example, a typical RF switch can provide about 25-30 dB of isolation in the "off" state, so that each path with two switches provides about 50-60 dB of isolation. The leakage, though relatively small, can result in varying DC offsets from the AQDS 110 for the phase shifter settings. In one embodiment, the ACPCE circuit 118 activates the ground switch control 172 for each phase shifter setting to characterize and compensate for the DC offset for different phase shifter settings.

Please replace the paragraph starting on page 35, line 14 with the following amended paragraph:

The QMCSP [[510]] 1510 receives the control interface 1514, which includes the data to be quadrature modulated, and processes the data to compensate for quadrature impairment in the digital-to-analog converters 130, 132, the reconstruction filters 134, 136, and the analog

quadrature modulator 138. The QMCSP 1510 compensates for quadrature impairment in real time. In a typical telecommunications application, such as W-CDMA, the QMCSP 1510 processes signals at a relatively fast rate. In one embodiment, the signal processing in the QMCSP 1510 is performed by dedicated hardware such as a field programmable gate array (FPGA), such as an FPGA or other programmable logic device, which are available from sources such as Xilinx, Inc. or Altera Corporation. In one embodiment, the QMCSP 1510 is implemented within an application specific integrated circuit (ASIC).

Please replace the paragraph starting on page 36, line 30 with the following amended paragraph:

Figure 16 illustrates an alternative embodiment 1600 of a portion of the Analog Quadrature Modulator/Demodulator System 100 according to the present invention. In the alternative embodiment 1600 shown in Figure 16, the ACPCE monitors the digital compensated signal 126, 128 rather than the input signal 122, 124, the ACPCE monitors the received ~~bandwidth~~ baseband signals 160, 162 rather than the demodulated baseband signals 164, 166, and injects test signals to the inputs of the AQMS 104 rather than through the inputs of the QMCSP 102. Of course, combinations of the features from the embodiments shown in Figures 1 and 16 are also possible.

Please replace the paragraph starting on page 42, line 3 with the following amended paragraph:

The QDCSP 1900 includes an I-to-I compensation filter 1902, an I-to-Q compensation filter 1904, a Q-to-Q compensation filter 1906, an in-phase DC offset register 1908, a quadrature phase DC offset register [[1914]] 1910, an in-phase adder 1912, a first quadrature-phase adder 1914, and a second quadrature-phase adder 1916. The ACPCE circuit 118 provides coefficients and values to the compensation filters 1902, 1904, 1906 and the offset registers 1908, 1910 through update vectors 1924, 1926, 1928, 1930, 1932 of the demodulator state parameter update vector 170, respectively.

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Please replace the paragraph starting on page 42, line 15 with the following amended paragraph:

The first quadrature-phase adder 1914 sums the quadrature-phase portion of the received baseband signal 162 with the value stored in the quadrature-phase DC offset register 1910, and applies the summation as an input to the Q-to-Q compensation filter 1906. The outputs of the I-to-Q compensation filter 1904 and the Q-to-Q compensation filter 1906 are summed by the second quadrature-phase adder 1916 to generate the quadrature phase of the demodulated baseband signal 166. Of course, where implemented by firmware, the demodulated baseband signals 164, 166 can be maintained within a memory device accessed by the firmware.